2. (Amended Once) The method of claim 1, wherein the multiple step voltage pulse comprises:

applying the first voltage pulse for a first time interval; and

applying the second voltage pulse for a second time interval;

wherein the first and second time intervals are substantially coincident[al] with applying the voltage pulse at the source of the semiconductor device.

A1 cont'd

5. (Amended Once) The method of claim 1, wherein the voltage pulse at the source of the semiconductor device [further] comprises applying [the voltage pulse] for a third time interval.

A2

16. (Amended Once) The method of claim 1, wherein the voltage pulse at the source of the semiconductor device further comprises:

applying a third voltage pulse for a first time interval; and

applying a substantially identical fourth voltage pulse for a third [second] time interval;

wherein the first time interval and the third [second] time interval are separated by a second [third] time interval during which no voltage [pulse] is applied to the source of the semiconductor device.

A3

18. (Amended Once) The method of claim 16, wherein the first time interval is substantially identical to the third [second] time interval.

A4

19. (Amended Once) The method of claim 16, wherein the first time interval and the third [second] time interval are greater than the second [third] time interval.

22. (Amended Once) The method of claim 16, wherein the multiple step voltage pulse at the gate of the semiconductor device comprises:

applying the first voltage pulse for a fourth time interval; and

applying the second voltage pulse for a sixth [fifth] time interval;

wherein the first voltage pulse and the second voltage pulse are separated by a fifth [sixth] time interval during which no voltage [pulse] is applied to the gate of the semiconductor device.

A5

A

26. (Amended Once) A method for erasing a semiconductor device comprising:

applying a constant positive voltage pulse for a first time interval at the source of the semiconductor device;

applying a first negative voltage pulse for a second time interval at the gate of the semiconductor device; and

applying a second negative voltage pulse for a third time interval at the gate of the semiconductor device;

A4 wherein said second negative voltage pulse [step] is greater in magnitude than said first negative voltage pulse [step].

27. (Amended Once) The method of claim 26 [22], wherein the constant positive voltage pulse is about 5.0 V.

28. (Amended Once) The method of claim 26 [22], wherein the first negative voltage pulse is about –5.0 V and the second negative voltage pulse is about –10.0 V.

Please amend the Abstract of the Disclosure as follows:

In one aspect, the present invention provides a method for erasing a semiconductor device that comprises applying a voltage pulse at the source of the semiconductor device and a multiple step voltage pulse of the opposite polarity at the gate of the semiconductor device. The multiple step voltage pulse comprises at least a first voltage pulse and a second voltage pulse at the gate of the semiconductor device. The second voltage pulse is usually greater in magnitude

A7 than the first voltage pulse. [ ] In another aspect, the present invention provides a method for erasing a semiconductor device that comprises applying a substantially constant positive voltage pulse for a first time interval, t_1, at the source of the semiconductor device. A first and then a second negative voltage pulse are also applied at the gate of the semiconductor device for a second and third time interval, t_2 and t_3, respectively. The second negative voltage pulse is greater in magnitude than the first negative voltage pulse. The negative and positive voltage pulses are substantially coincident[al] in time.

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